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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,227	12/02/2003	Mark Jackson Pulver	PEA27US	4605
24011	7590	10/19/2006	EXAMINER	
SILVERBROOK RESEARCH PTY LTD 393 DARLING STREET BALMAIN, NSW 2041 AUSTRALIA			MRUK, GEOFFREY S	
			ART UNIT	PAPER NUMBER
			2853	

DATE MAILED: 10/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/727,227

Applicant(s)

JACKSON PULVER ET AL.

Examiner

Geoffrey Mruk

Art Unit

2853

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 02 October 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1 and 20-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 20-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2 October 2006 has been entered.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1 states, "wherein the integrated circuit comprises a plurality of first and second reticle exposed areas in sequential arrangement, each first reticle exposed area having nozzle logic circuitry and each second reticle exposed area having connection pads for connecting the nozzle logic circuitry to power and data, wherein a first end of each first reticle exposed area is

configured to interconnect with either a second end of an adjacent first reticle exposed area or a first end of an adjacent second reticle exposed area and the second end of each first reticle exposed area is configured to interconnect with either the first end of an adjacent first reticle exposed area or a second end of an adjacent second reticle exposed area.” Applicant seems to be claiming features within the integrated circuit, i.e. logic circuitry and pads. However, the examiner is not sure to what the metes and bounds of the claimed invention is since the written description at paragraphs 4243 to 4355 and 4367 to 4370 fail to describe the final CMOS/MEMS structure as a result of the process steps disclosed. Paragraphs 4243 to 4355 merely add an aggregate listing of printing terminology. Further, the specification does not provide a figure showing the final CMOS/MEMS structure. Therefore, based upon an inadequate disclosure, one of ordinary skill in the art would not be able to ascertain the final integrated circuit structure or the arrangement of the first and second areas once the reticle layout is removed.

2. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter that was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 1 states, “wherein the integrated circuit comprises a plurality of first and second reticle exposed areas in sequential arrangement, each first reticle exposed area having nozzle logic circuitry and each second reticle exposed area having connection pads for connecting the nozzle logic circuitry to power and data, wherein a first end of each first reticle exposed area is configured to interconnect with either a second end of an

adjacent first reticle exposed area or a first end of an adjacent second reticle exposed area and the second end of each first reticle exposed area is configured to interconnect with either the first end of an adjacent first reticle exposed area or a second end of an adjacent second reticle exposed area.” Applicant seems to be claiming process steps for exposing areas on a chip. However, the examiner is not sure to what the metes and bounds of the claimed invention is since the written description at paragraphs 4367 to 4370 fail to describe the details of each process step. For example, in paragraph 4368, what does “stitch” or “overlapping” mean? Further, figure 323 fails to label the “top” and “bottom” of each respective area. Therefore, one of ordinary skill in the art would not be able to make an integrated circuit with the disclosed process steps.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1 and 21-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite in that it fails to point out what is included or excluded by the claim language. This claim is an omnibus type claim. Claim 1 recites the limitation “wherein the integrated circuit comprises a plurality of first and second reticle exposed areas in sequential arrangement, each first reticle exposed area having nozzle logic circuitry and each second reticle exposed area having connection pads for connecting the nozzle logic circuitry to power and data, wherein a first end of each first reticle exposed area is configured to inter connect with either a second end of an adjacent first reticle exposed

Art Unit: 2853

area or a first end of an adjacent second reticle exposed area and the second end of each first reticle exposed area is configured to interconnect with either the first end of an adjacent first reticle exposed area or a second end of an adjacent second reticle exposed area.” There resides no the final CMOS/MEMS structure in the claims that determines what is included and not included in the invention. Therefore, one of ordinary skill in the art would not be able to ascertain the metes and bounds of the term “wherein the integrated circuit comprises a plurality of first and second reticle exposed areas in sequential arrangement, each first reticle exposed area having nozzle logic circuitry and each second reticle exposed area having connection pads for connecting the nozzle logic circuitry to power and data, wherein a first end of each first reticle exposed area is configured to inter connect with either a second end of an adjacent first reticle exposed area or a first end of an adjacent second reticle exposed area and the second end of each first reticle exposed area is configured to interconnect with either the first end of an adjacent first reticle exposed area or a second end of an adjacent second reticle exposed area.”

2. Claims 21-24 are rejected under 35 U.S.C. 112, second paragraph, for being dependent upon a claim with the above addressed 35 U.S.C. 112 problems (i.e. claim 1).

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Jarrold et al. (US 2002/0093548 A1).

With respect to claim 1, Jarrold discloses a printhead integrated circuit incorporating microelectromechanical inkjet nozzle systems (MEMS), wherein the integrated circuit comprises a plurality of first and second reticle exposed areas in sequential arrangement, each first reticle exposed area having nozzle logic circuitry (paragraphs 0004, 0047) and each second reticle exposed area having connection pads for connecting the nozzle logic circuitry to power and data (paragraph 0024, elements 30, 32), wherein a first end of each first reticle exposed area is configured to interconnect with either a second end of an adjacent first reticle exposed area or a first end of an adjacent second reticle exposed area and the second end of each first reticle exposed area is configured to interconnect with either the first end of an adjacent first reticle exposed area or a second end of an adjacent second reticle exposed area.

***Response to Arguments***

Applicant's arguments filed 24 August 2006 have been fully considered but they are not persuasive. The applicant's argument that "independent claim 1 is amended to be directed to a printhead integrated circuit, to clarify that the first and second reticle exposed areas are sequentially arranged, that the first areas having inkjet nozzle logic circuitry, that the second areas have connection pads for connecting power and data to the nozzle logic, and to specify that the ends of the first and second areas are configured to be interconnect able in the manner claimed. Support for these amendments can be found, for example, at paragraphs 4243-4355 and 4367-4370 of the present specification" is not persuasive. As stated in the instant rejection, paragraphs 4243 to 4355 merely add an aggregate listing of printing terminology. Further, the specification does not provide a figure showing the final CMOS/MEMS structure while the written description at paragraphs 4367 to 4370 fail to describe the details of each process step. Therefore, based upon an inadequate disclosure, one of ordinary skill in the art would not be able to ascertain the final integrated circuit structure, the arrangement of the first and second areas once the reticle layout is removed, and be able to make an integrated circuit with the disclosed process steps.



***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Geoffrey Mruk whose telephone number is 571 272-2810. The examiner can normally be reached on 7am - 330pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Meier can be reached on 571 272-2149. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GSM  
10/12/2006



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